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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/812,830      | 03/29/2004  | Robert Bergmann      | E0196.0006          | 3112             |

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EXAMINER

ABOAGYE, MICHAEL

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

1725

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                               |                                 |  |
|------------------------------|-------------------------------|---------------------------------|--|
| <b>Office Action Summary</b> | Application No.<br>10/812,830 | Applicant(s)<br>BERGMANN ET AL. |  |
|                              | Examiner<br>Michael Aboagye   | Art Unit<br>1725                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>04/16/2004</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites " a second gas channel which points away from the plate in a direction within two-dimensional extent of the plate". It is unclear what is being claimed, and therefore is vague and indefinite. Clarification and /or correction are required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (US Patent No. 5,984,165).

Regarding claim 1- 3, Inoue et al. discloses a device for soldering contacts between an integrated semiconductor chips and a printed circuit board, comprising: an X-Y table ("20", figure 2) with suction openings for clamping and transporting the electronic board positioned above the clamping device ("1", figures 1 and 2; column 6,

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lines 16-26; a flushing device ("81", figure 2), a blowout passages (82, figure 2) for blowing either nitrogen purging or helium gas between the chip and the electronic board; two shield plates (80, figure 2) having an opening created therebetween (Note the examiner interprets the middle opening between the ends of the two shield plates as a window); said shield plates aligned parallel to the clamping device (figure 2); two channels formed within the shield plate for providing the flushing gas (83, figure 2); two gas outlets arranged in the window area, this is in reference to the wedge shaped channels between the proximal ends of the shield plate and the chip mount "30" (figure 2; column 8, lines 59-67, and column 9, lines 18-32); the chip mount positioned in the window and above the clamping device for applying pressure to the chip, this is in reference to the composite features ("50, 51 and 52", figure 1), a heater ("40", figure 2) for melting a solder applied to an underside of the chip (column 3, lines 1-14).

Regarding claims 4 and 5, Inoue et al. teaches a thermal radiation source, directed through the chip mount onto the chip said chip mount permeable to infra red radiation (figures 1 and 2, and columns column 3, lines 1-16).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

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the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Inoue et al. (US Patent No. 5,984,165) in view of Tsumura et al. (US Patent No. 6,288,376).

Inoue et al. teaches the limitation as set forth in claim 1 above, but do not expressly teach induction heating.

However Tsumura et al. discloses a method and device for melting a bump with a heater comprising an induction coil; an electrically conducting coil fitted into the solder so that the solder can be heated by an induction of eddy currents and causing the solder to melt (column 6, lines 32-41); said heating process requires no flux application, cleaning or drying resulting in enhanced bond integrity (Tsumura et al., abstract, column 2, lines 21-27).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have used an induction heating source in the method of Inoue et al. as taught by Tsumura et al. in order to ensure a clean solder melting process and achieving a bond with enhanced integrity (Tsumura et al., abstract, column 2, lines 21-27).

6. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosser et al. (GB 2,244,374) in view of Xie et al. (US Patent No. 6,334,567).

Rosser et al. teaches a method of connecting a semiconductor chips (21, figure 1 and abstract) onto the surface of a substrate wafer (13, figure and abstract), comprising the steps of: applying solder to the contact portion between the chip and the wafer; flushing the contacts of the chip and the component with a forming gas (page 6, lines 4); heating the chip from a side opposite the contact of the chip to melt the solder (figure 1); pressing the contact of the chip and the component onto one another and cooling the solder; wherein the chip is heated by a thermal radiation source ( page 3, paragraph 2); wherein the thermal radiation source is a laser radiation source (page 3, paragraph 3)

Rosser et al. does not expressly teach isothermal solidification.

However, Xie et al. teaches a soldering method for bonding together electronic components by heating and cooling the solder such that the solder undergoes isothermal solidification to forms a layer of a thickness 3-7 microns (Xie et al., abstract, column 1, lines 61- column 2, line 24; column 4, lines 49-56 and figure 1 &2).

It would have been obvious to one of ordinary skill in the art at the time the applicants invention was made to have used isothermal solidification in the soldering method of Rosser et al. as taught by Xie et al. in order to produce a solder layer of 3-7 microns at the joint portion between the two components (Xie et al., column 4, lines 49-56 and figure 1 &2).

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7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosser et al. (GB 2,244,374) in view of Xie et al. (US 6,334,567) as applied in claims 9 and 10 above and further in view of Hwang et al. (US 5,846,476).

Rosser et al. in view of Xie et al. do not expressly disclose and/or suggest a halogen lamp-heating source.

However, Hwang et al. teaches a method of connecting a silicon chip (20, figure 2) to a lead frame (24, figure 2) by using a halogen lamp heating source; said heating source lending it self to be adsorbed more by the silicon chip than the lead frame and thereby allowing selective heating to be achieved (Hwang et al. column 4, lines 35-40).

It would have been obvious to one of ordinary skill in the art at the time the applicants invention was made to have used a halogen lamp as the heating source in the method of Rosser et al. as modified by Xie et al. in view of the teachings of Hwang et al. in order to be able to conduct selective heating of components during an electronic assembly process (Hwang et al. column 4, lines 35-40).

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brownfield et al. (US 6,333,353), Sakuyama et al. (US 6,135,344), and Yamada (US 6,401,317) are also cited in PTO-892.


9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Aboagye whose telephone number is 571-272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

~~AM~~  
AM

  
Michael Aboagye  
Assistant Examiner  
Art unit 1725

10/13/2006

  
PATRICK JOSEPH RYAN  
SUPERVISORY PATENT EXAMINER